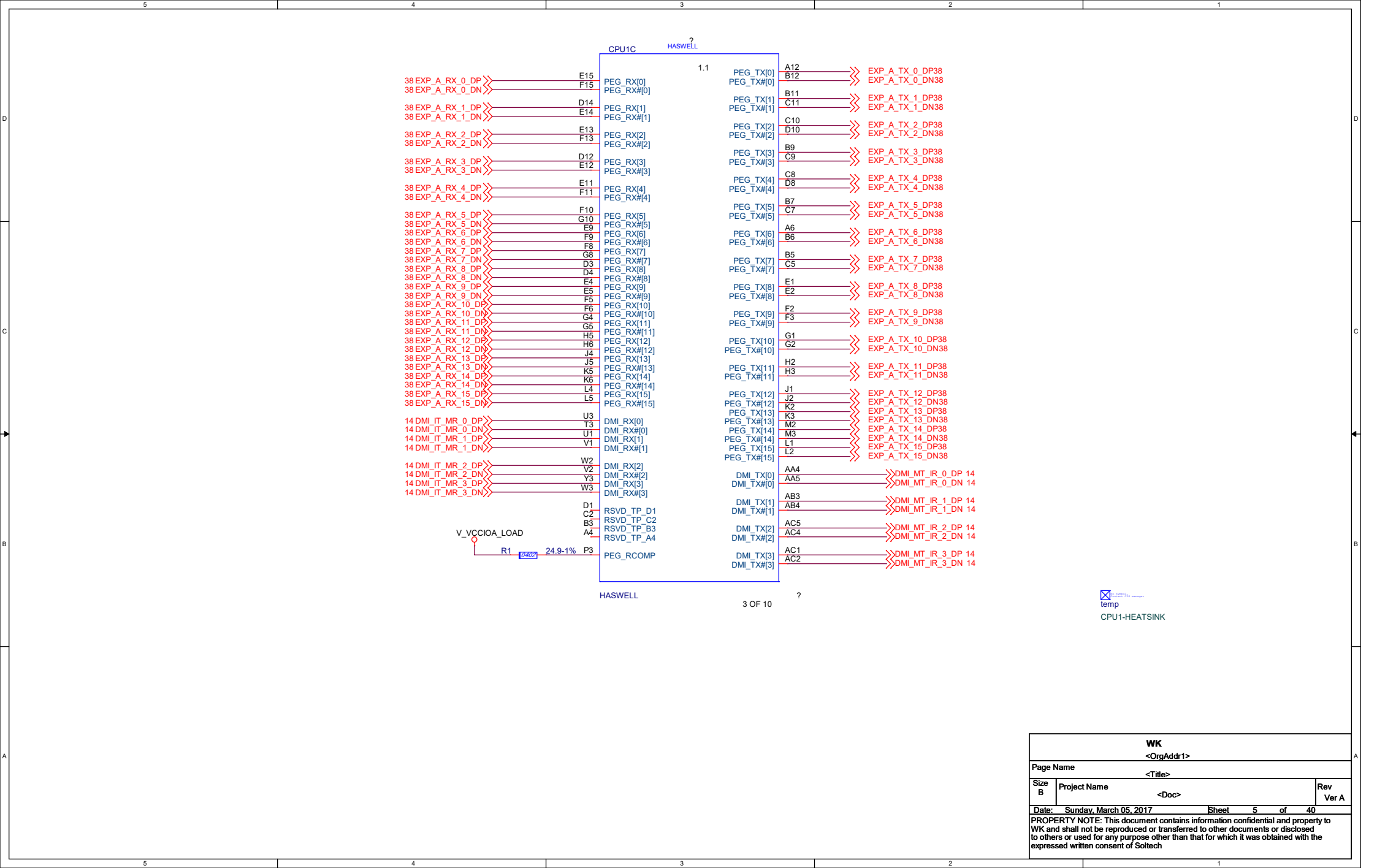
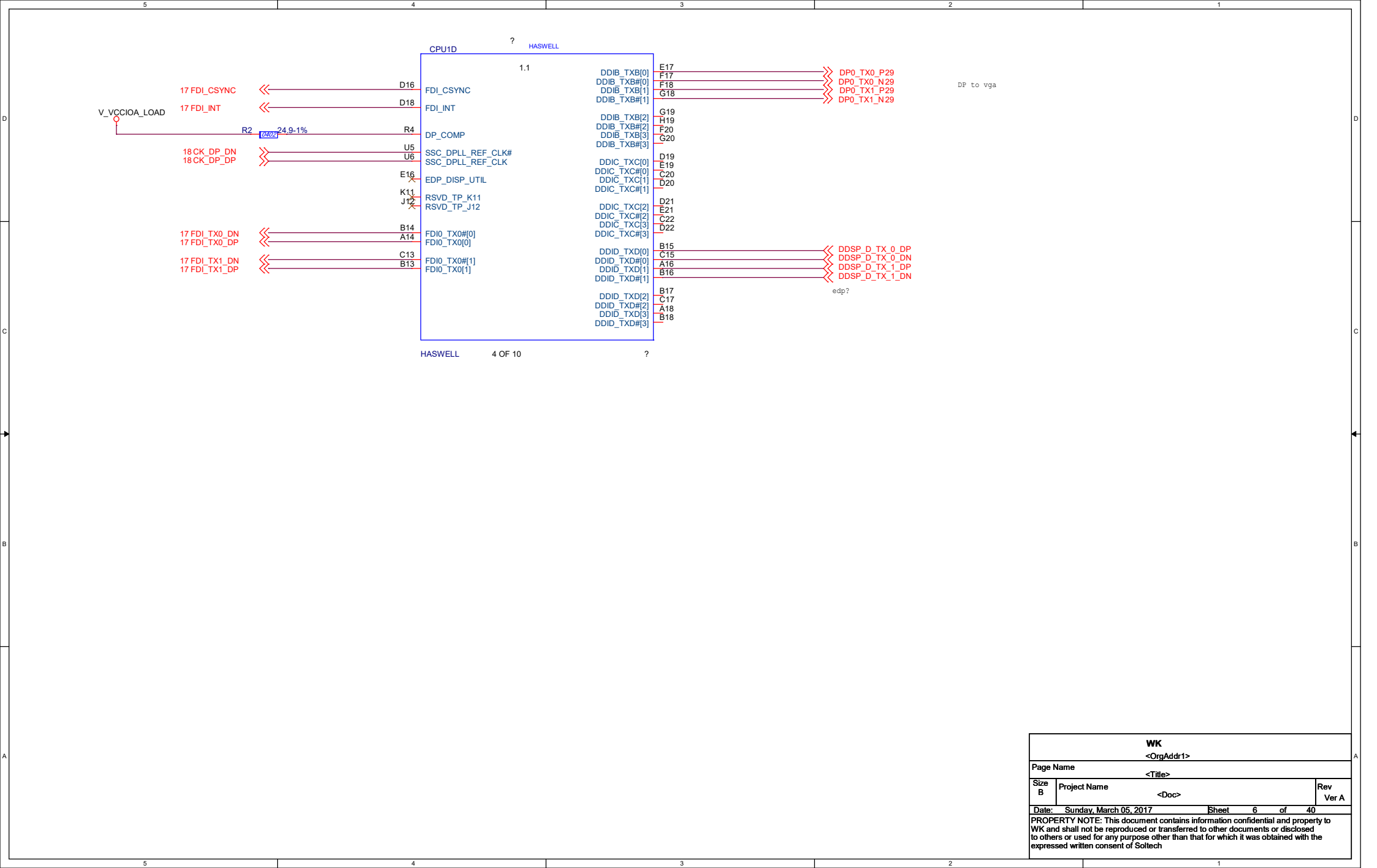
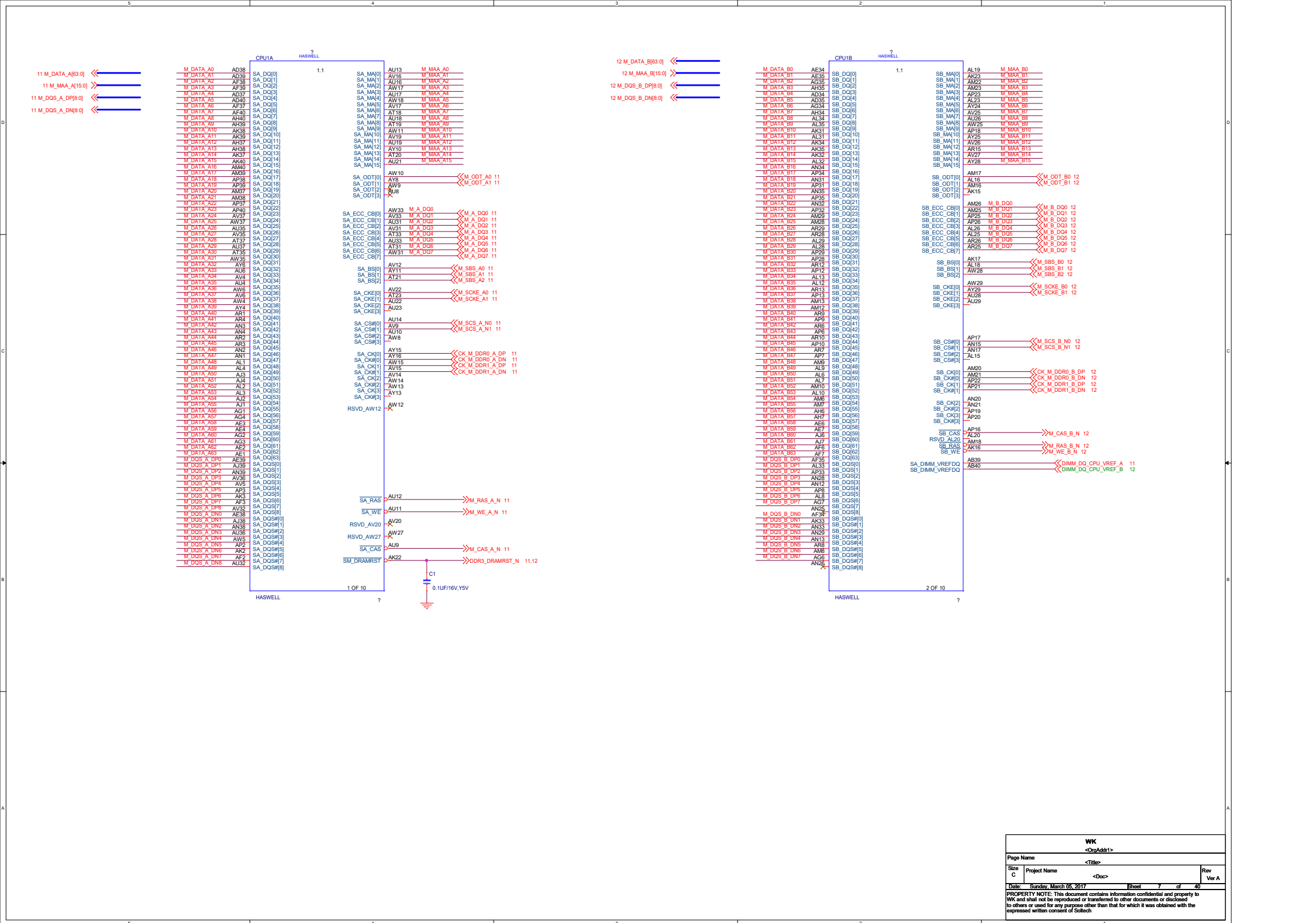
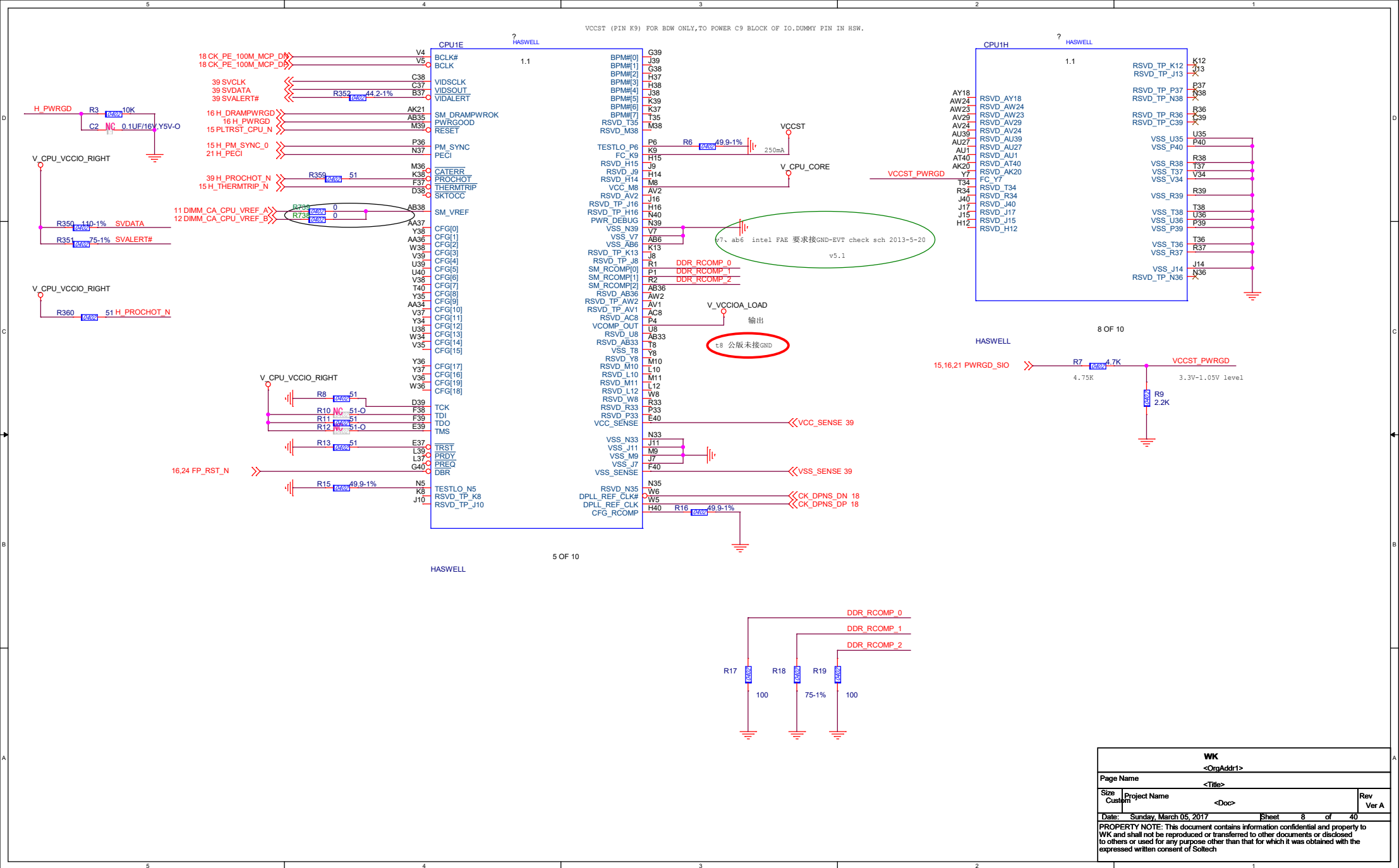


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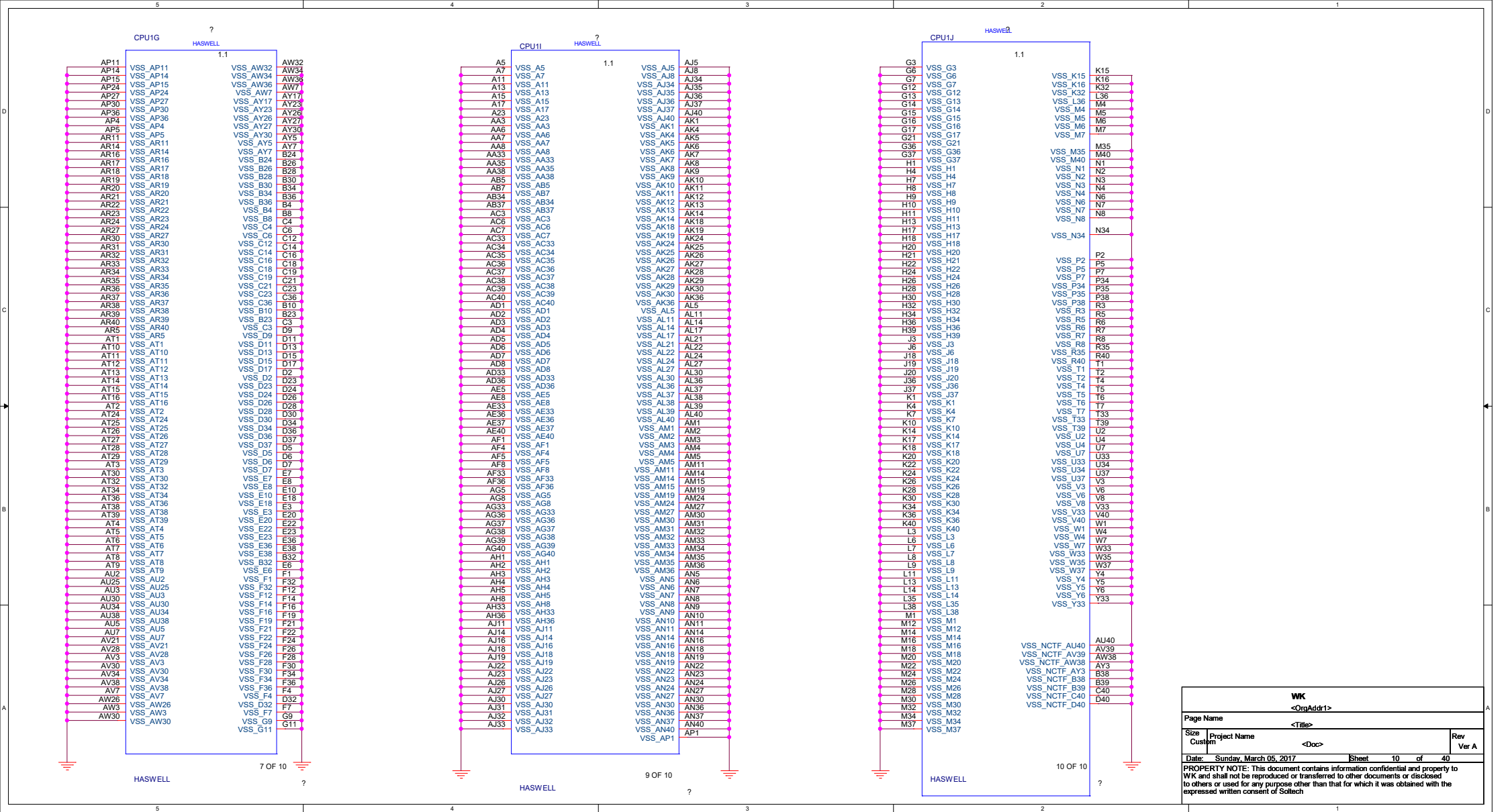




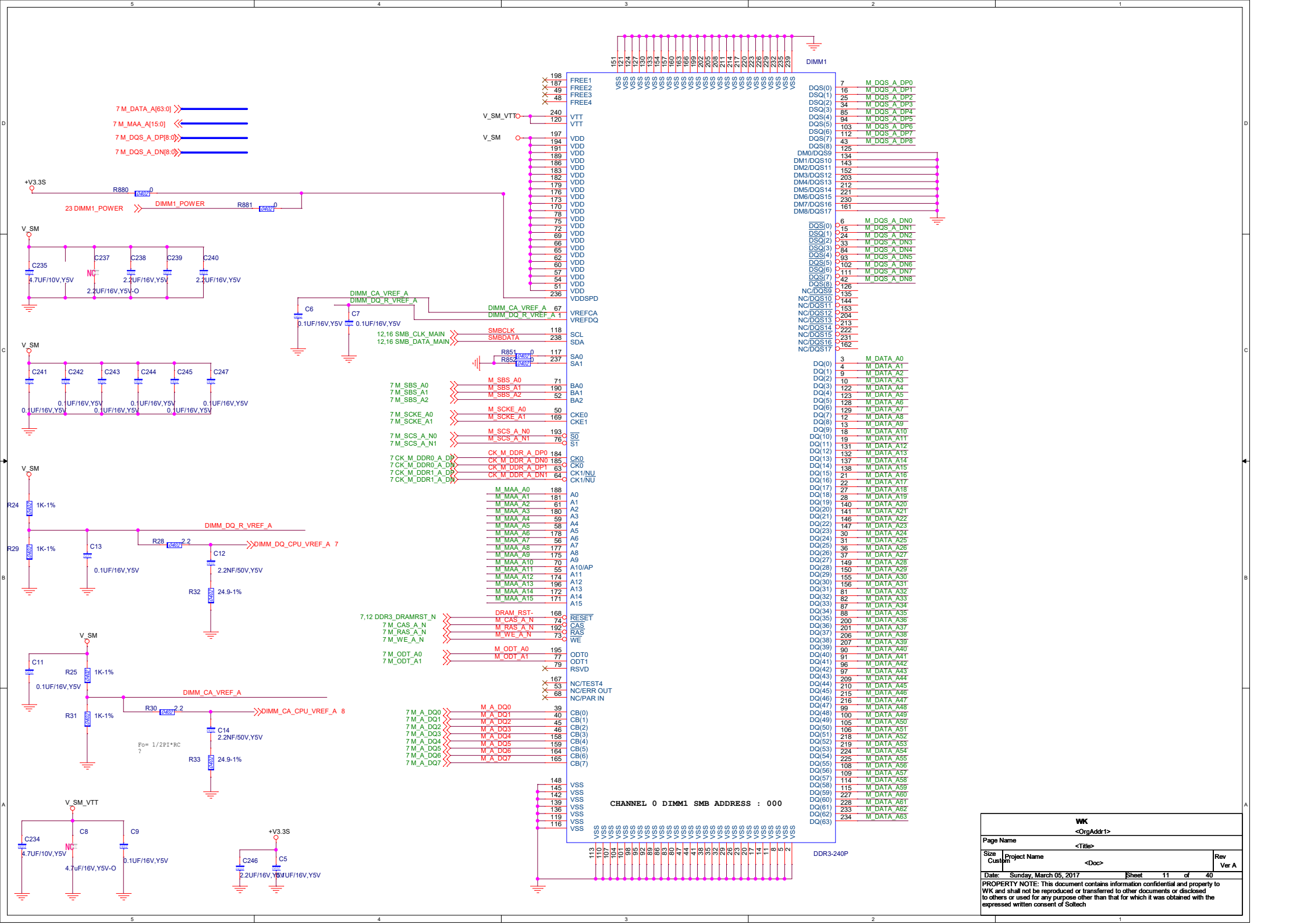


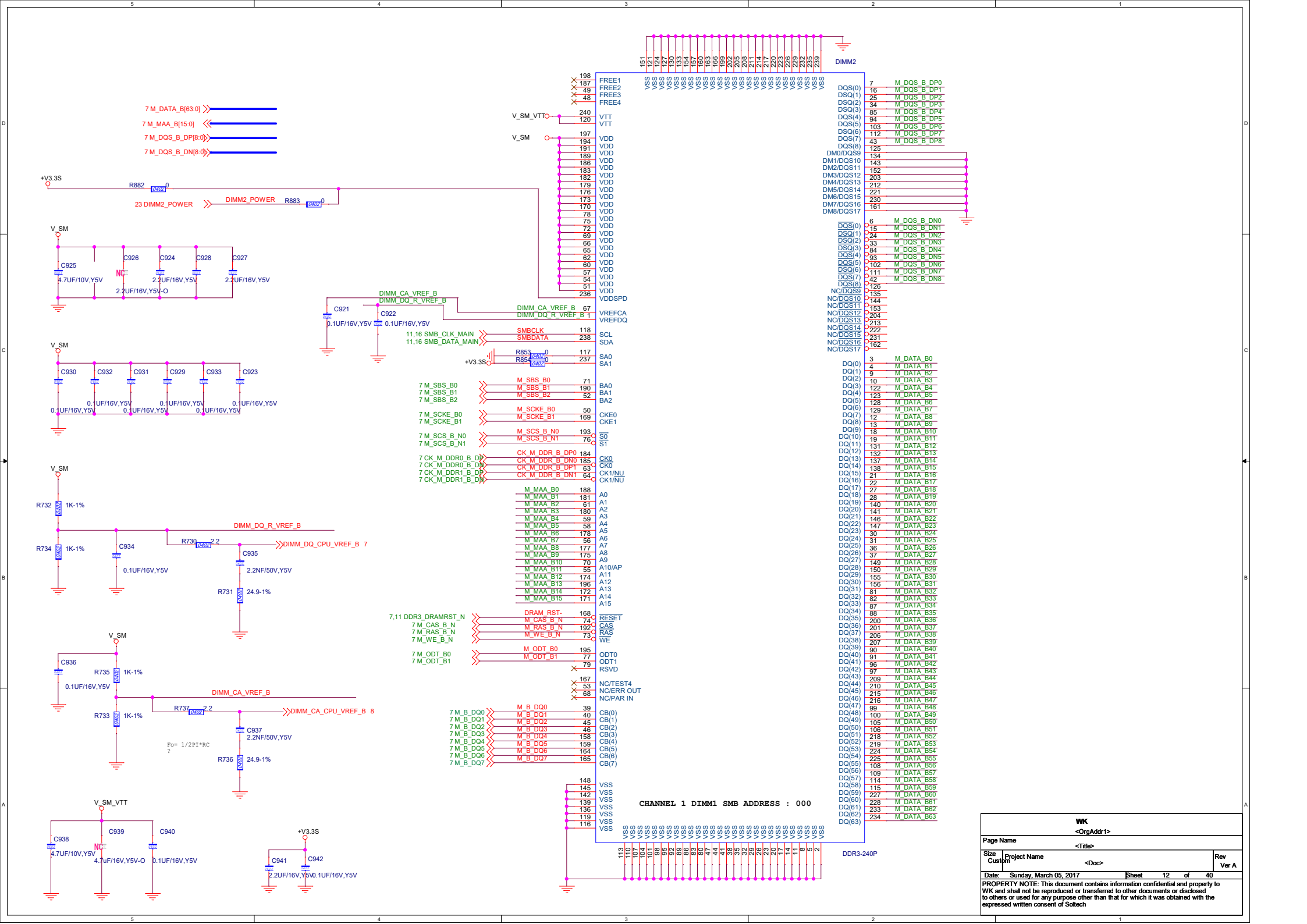


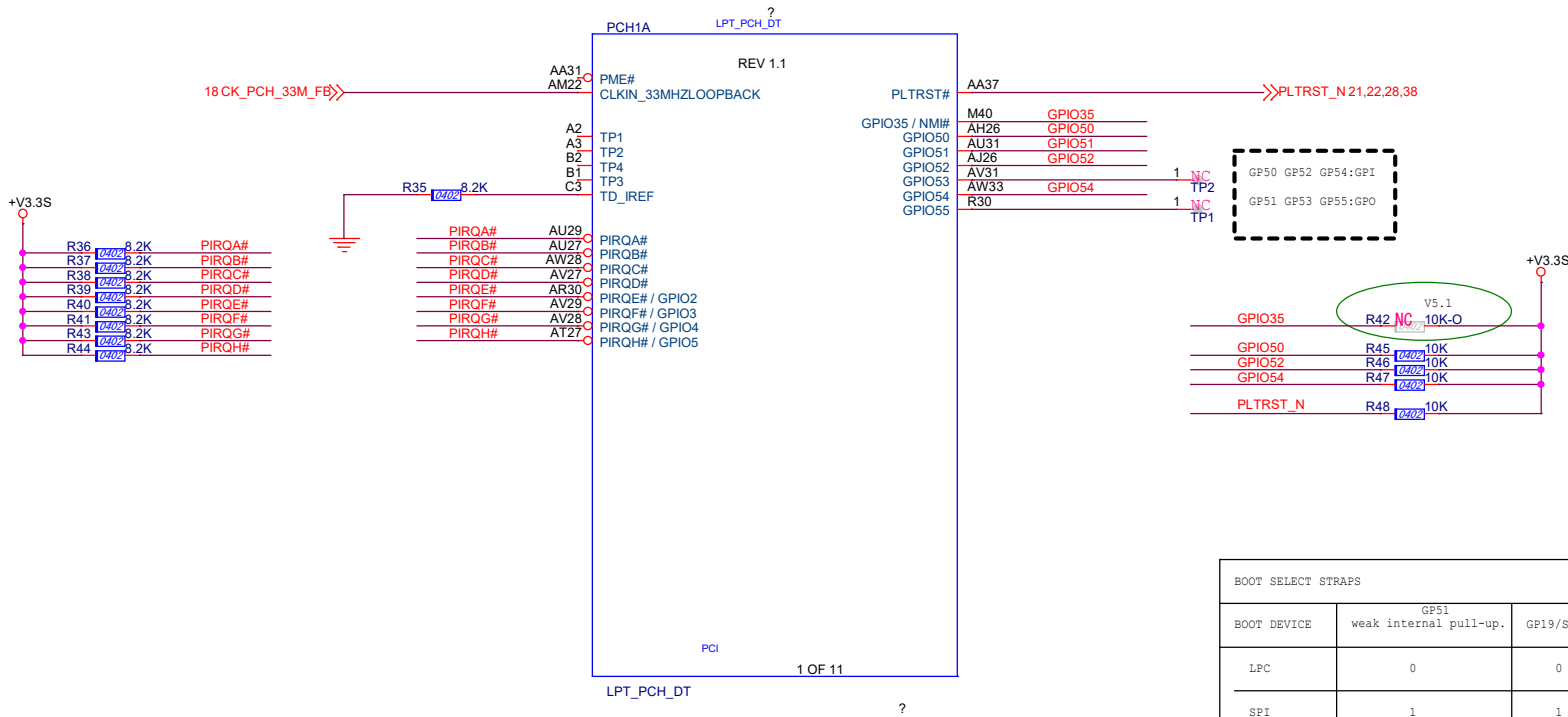












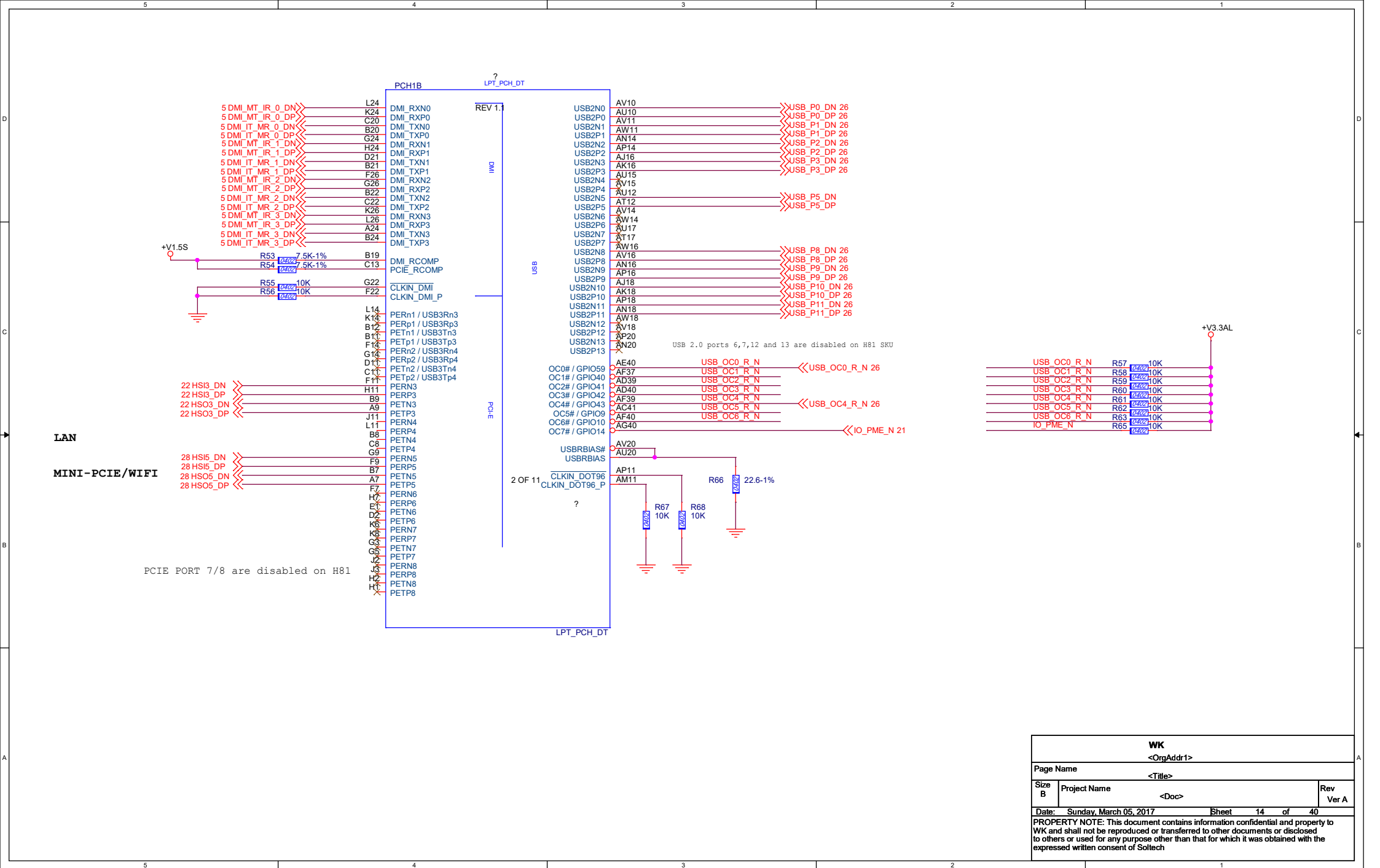
BOOT SELECT STRAPS		
BOOT DEVICE	GP51 weak internal pull-up.	GP19/SATA1GP
LPC	0	0
SPI	1	1

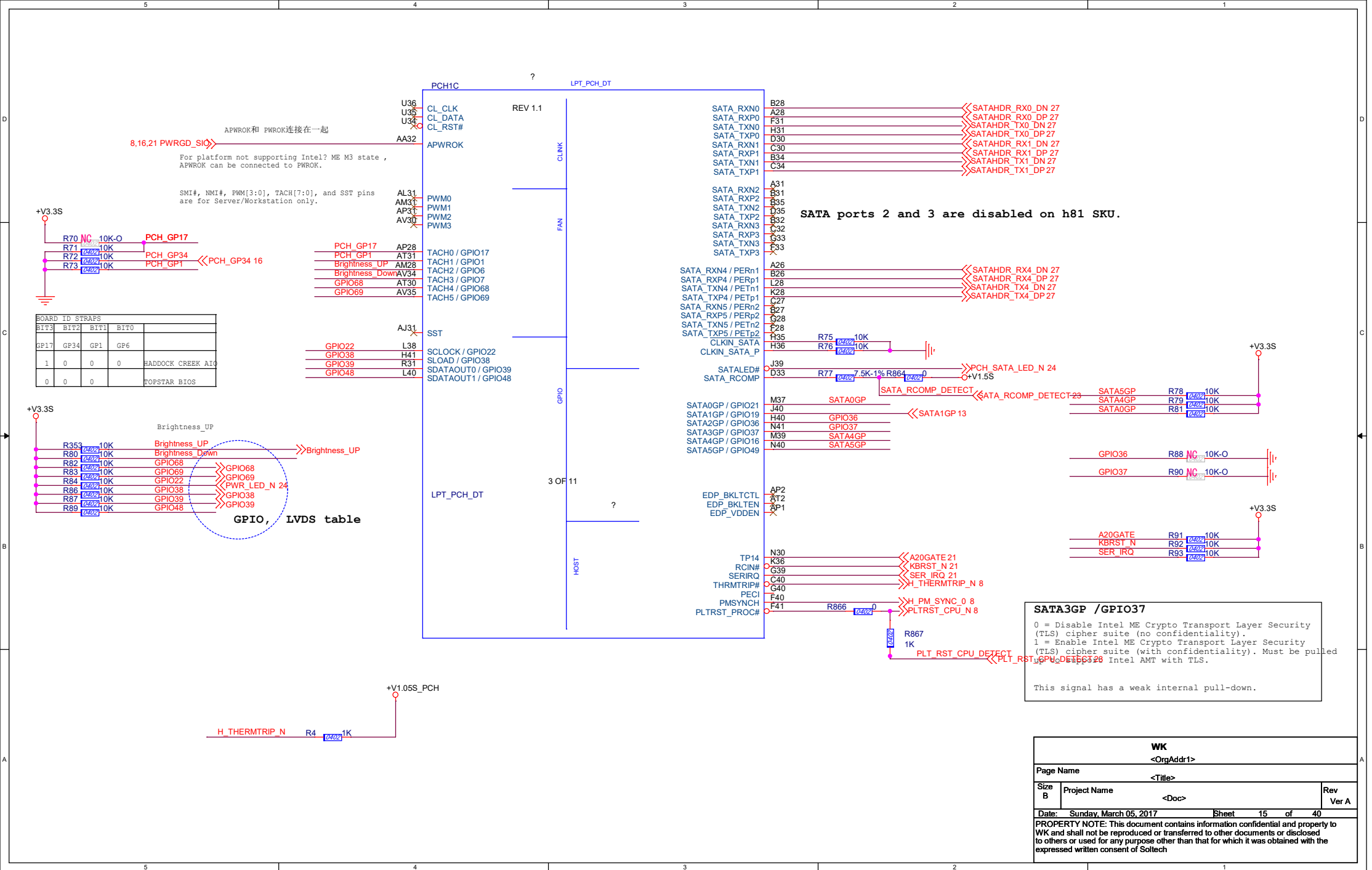
DMI AC-Coupling or DC-Coupling Mode

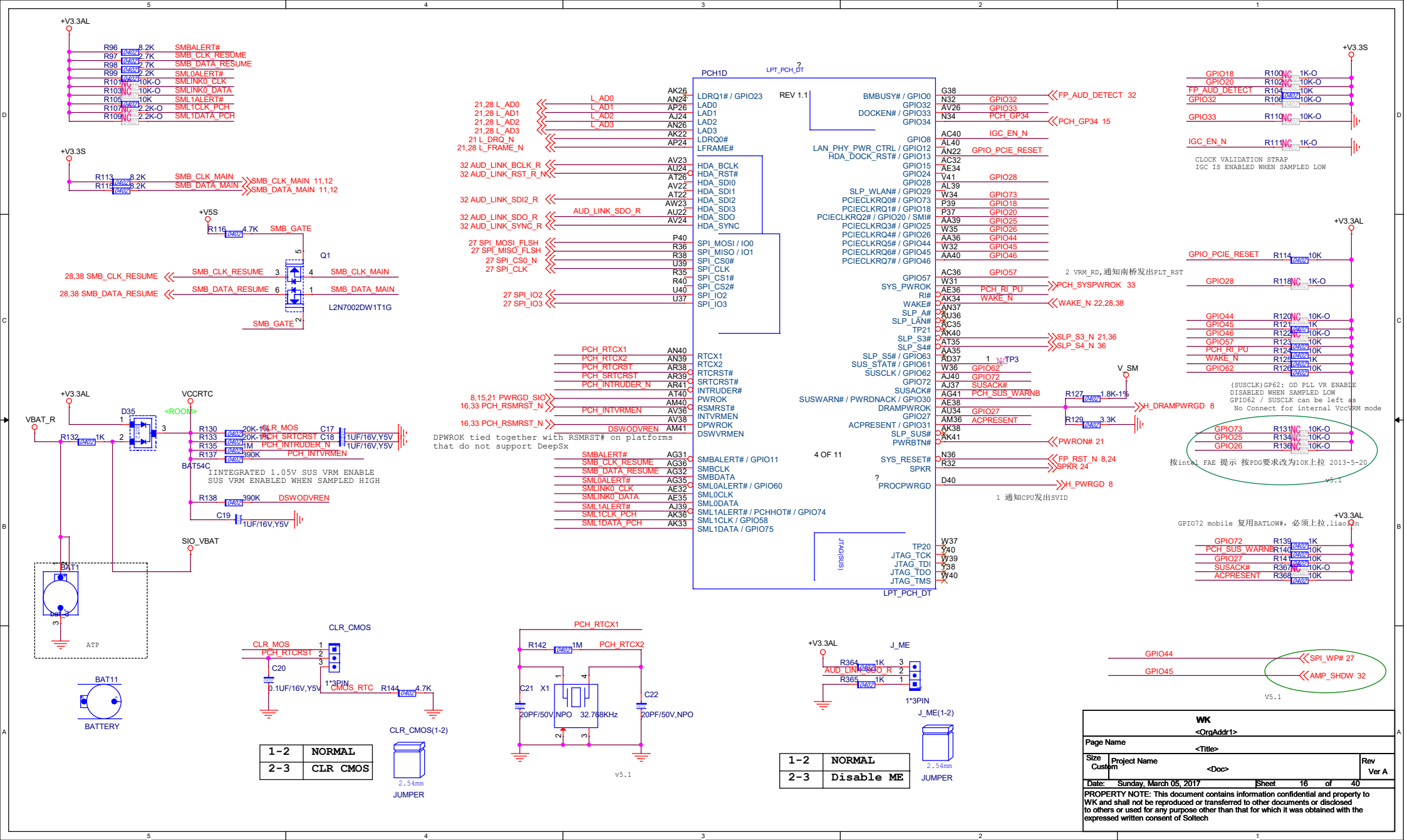
GPIO53	weak internal pull-up.
	0 = DMI is in AC-coupling mode (server/workstation only, not meant for desktop/mobile).
	1 = DMI is in DC-coupling mode (desktop, mobile or server/workstation).

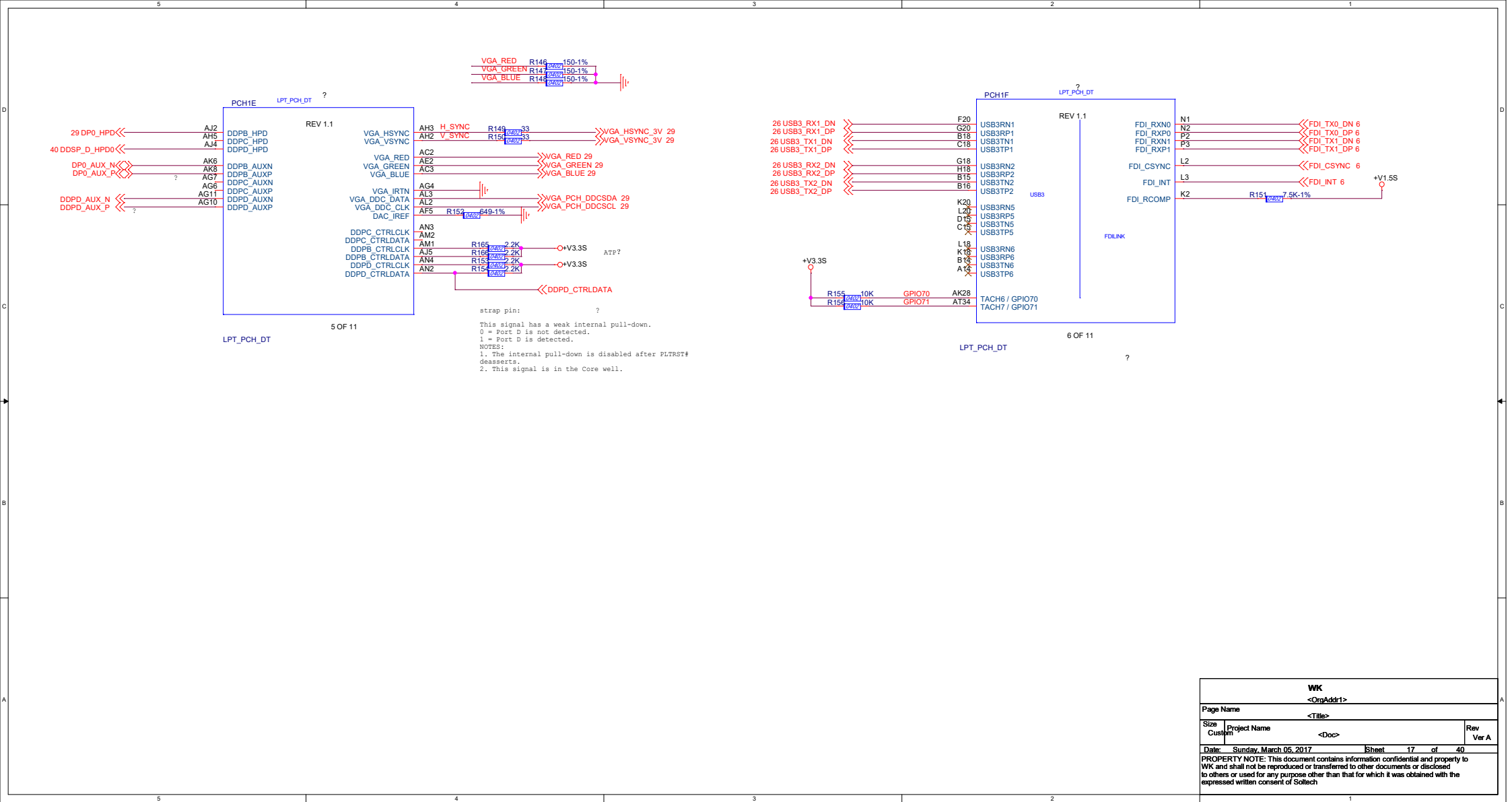
GPIO55 (weak internal pull-up)
A16 SWAP OVERRIDE OVERRIDE IF SAMPLED LOW

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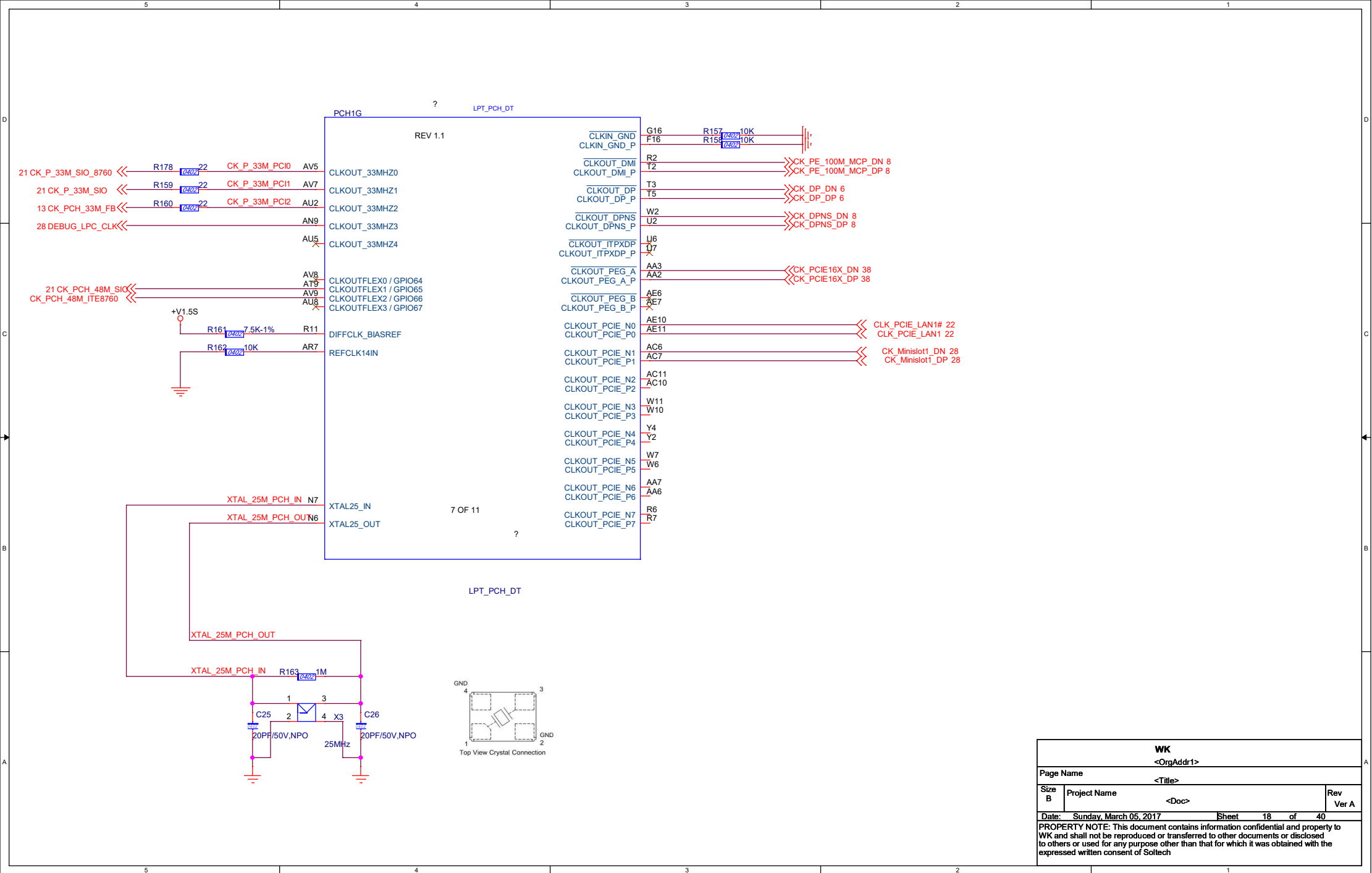








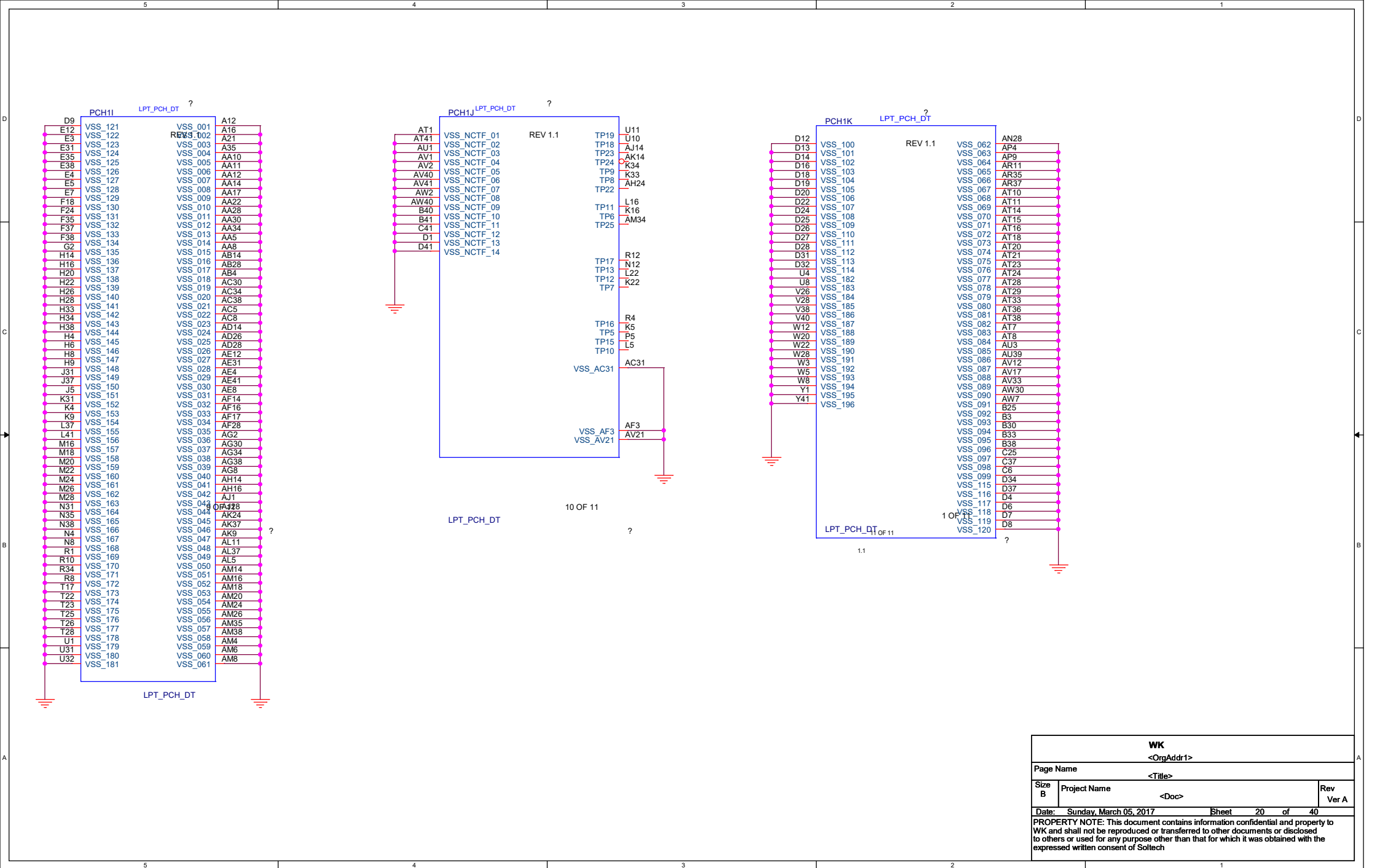
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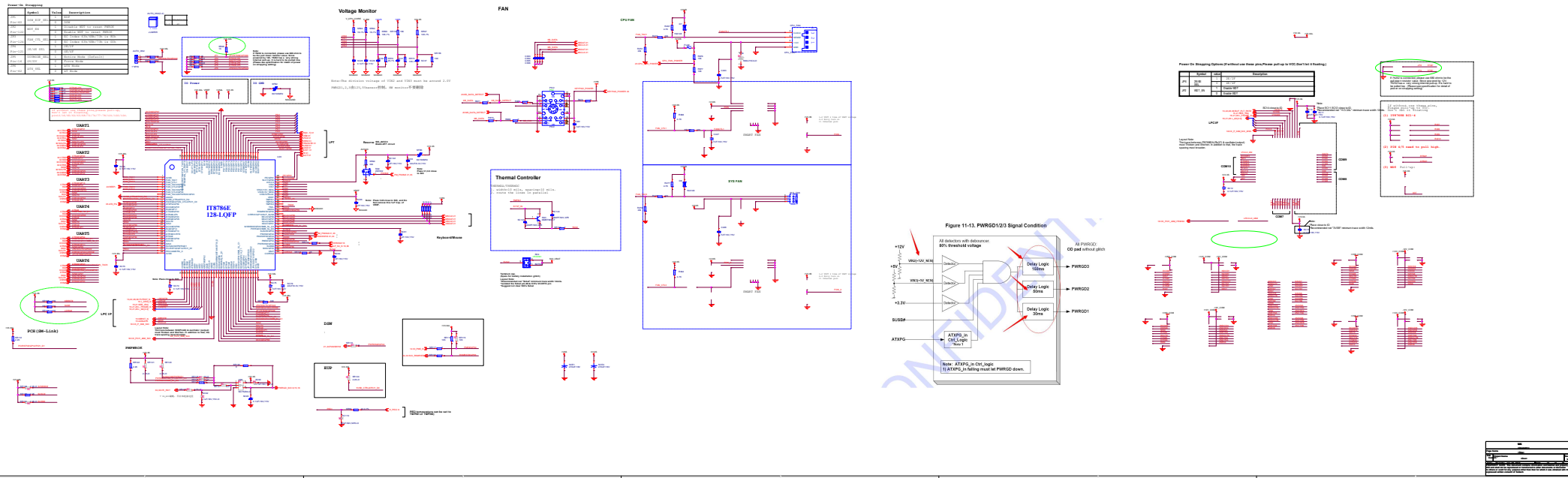


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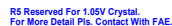
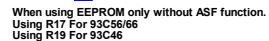




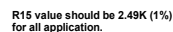




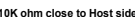
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1.4	2000-01-01	John Doe	John Doe
1.5	2000-01-01	John Doe	John Doe
1.6	2000-01-01	John Doe	John Doe
1.7	2000-01-01	John Doe	John Doe
1.8	2000-01-01	John Doe	John Doe
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2.0	2000-01-01	John Doe	John Doe



\* C23 are for VDD33/AVDD10\_XTAL pin-- 42

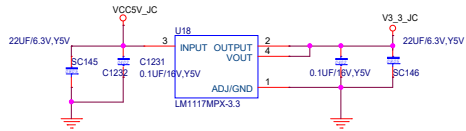
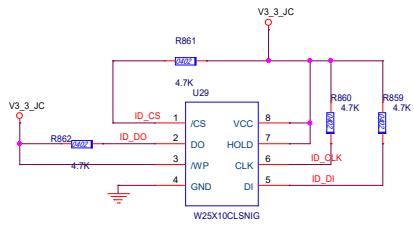


R285 For Enable Switch Regulator.  
R275 For Disable Switch Regulator

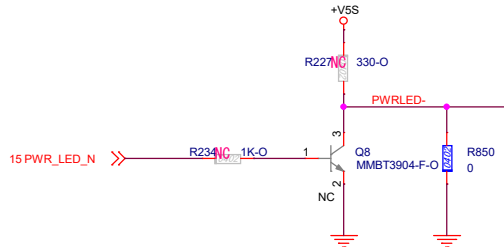
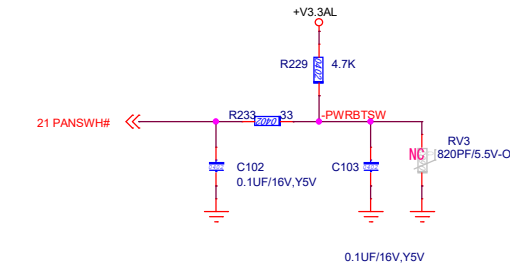
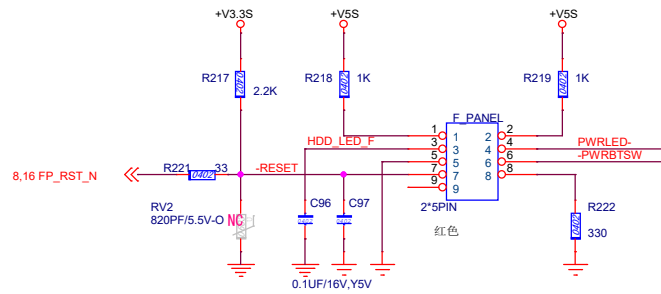
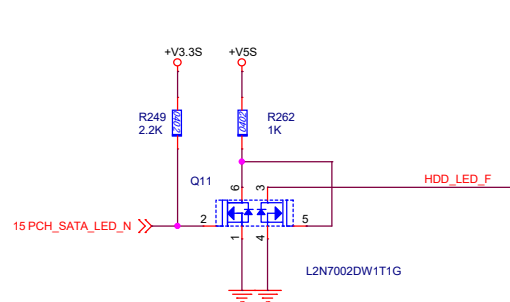
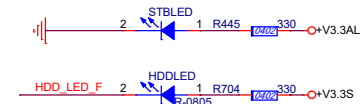
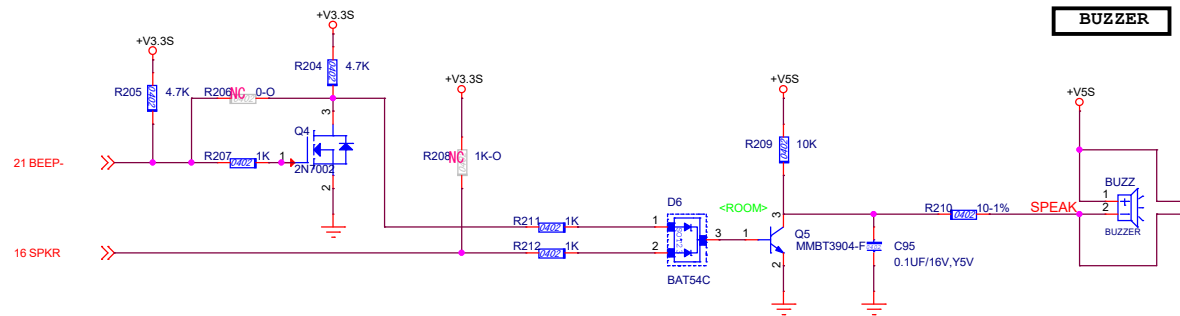


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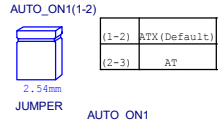
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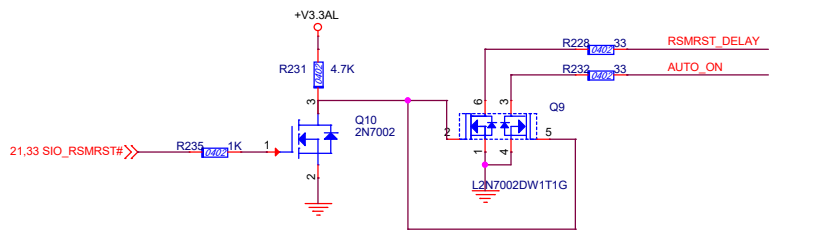
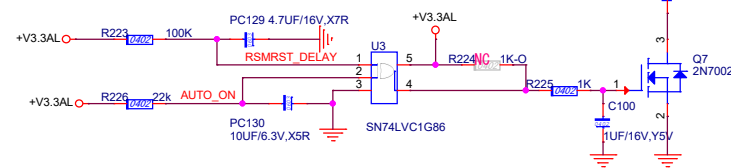
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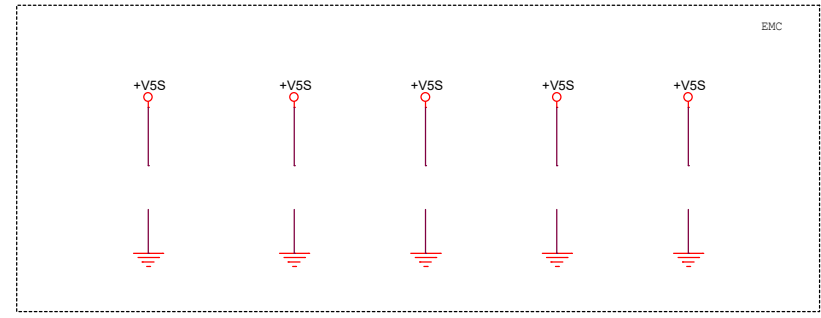
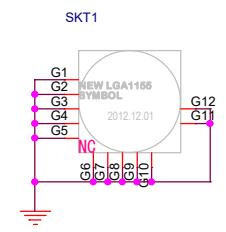
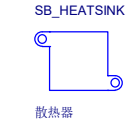
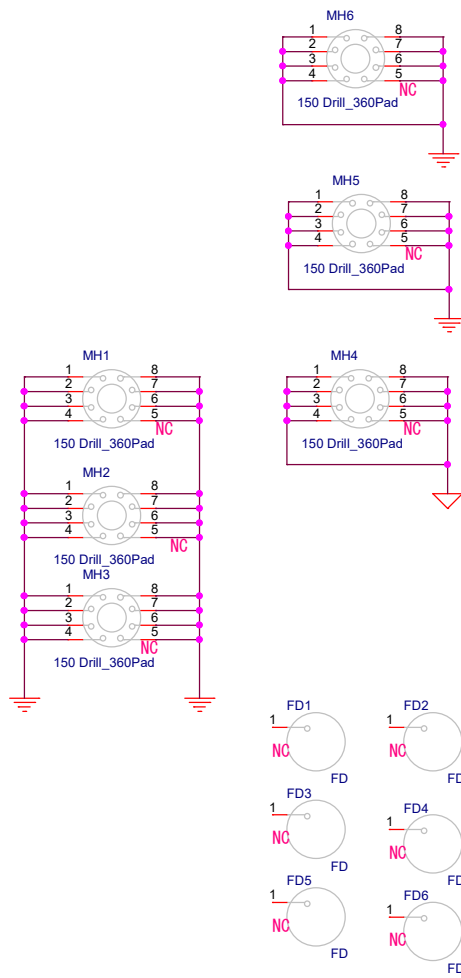
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异或门电路:  
自动上电电路模拟button 在RSMRST信号后给IO一个  
50~80ms的低电平信号。  
脉冲宽度以及产生时间通过R33 R34 C26 C27 调整



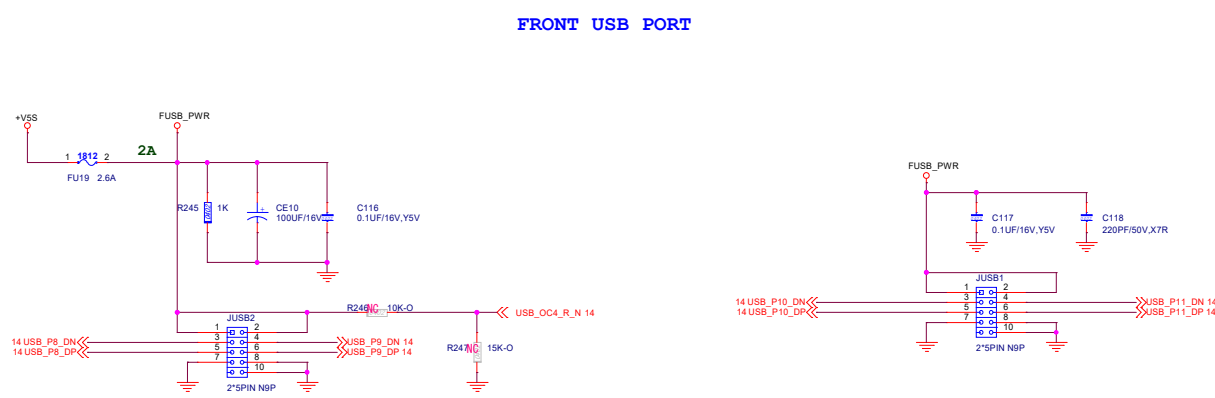
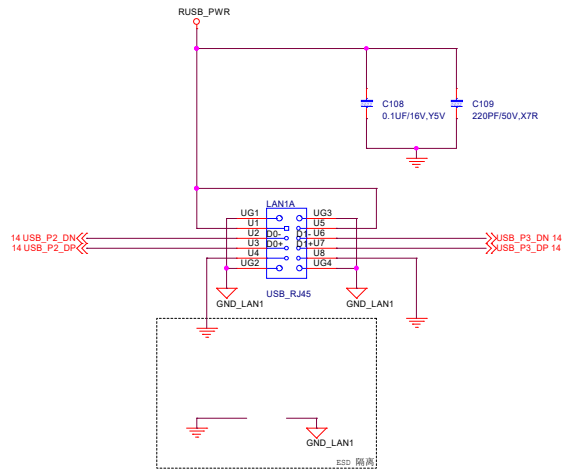
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L	L	L



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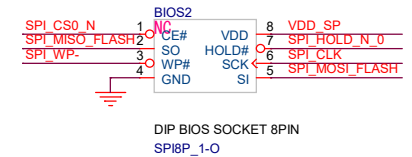
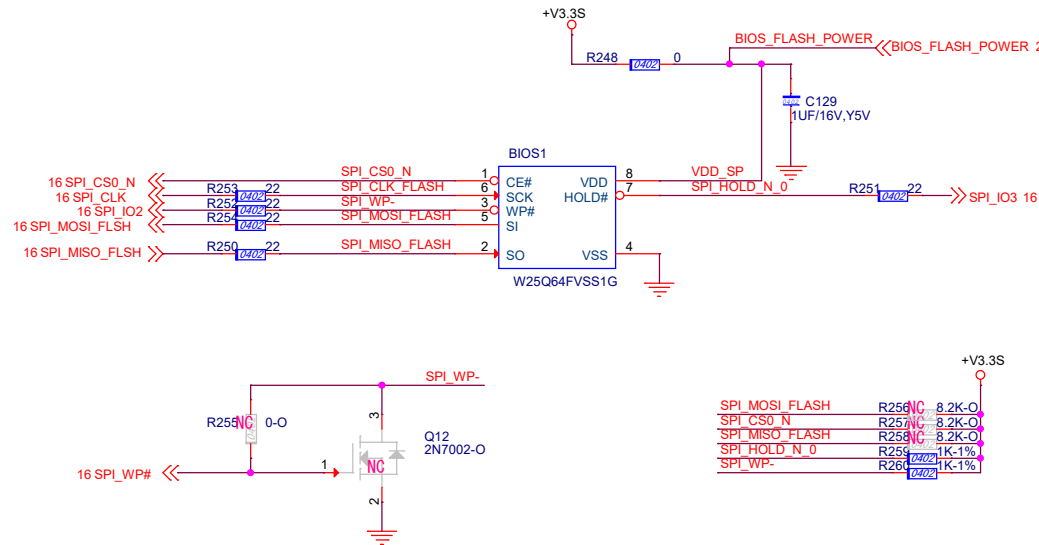
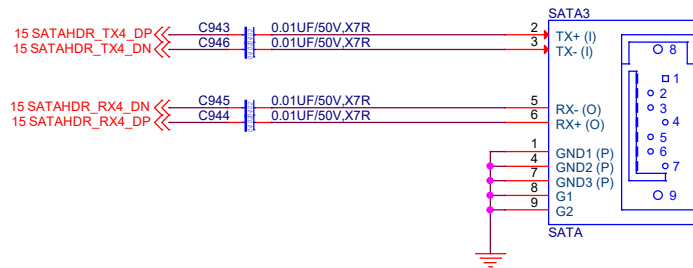
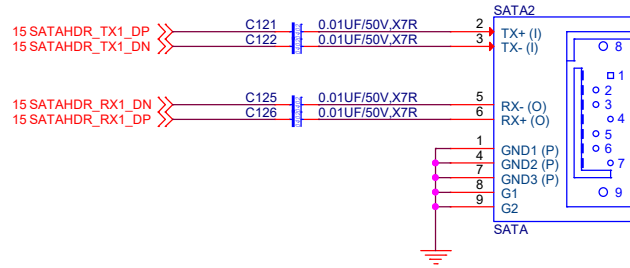
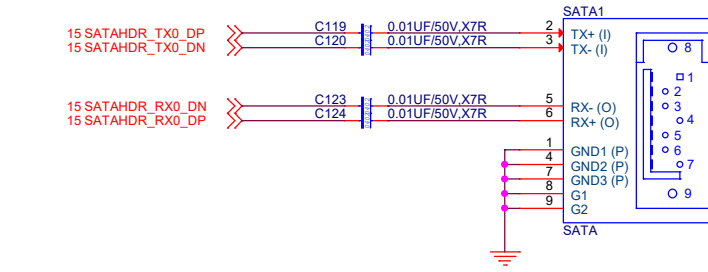
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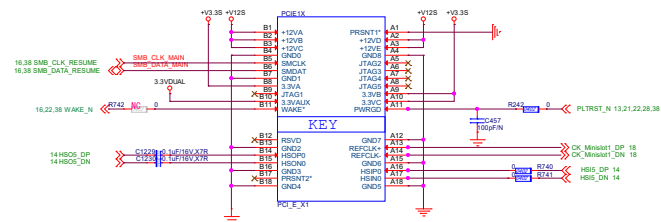
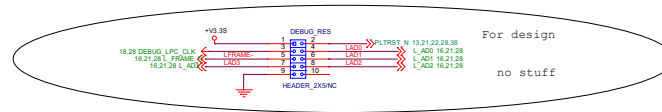
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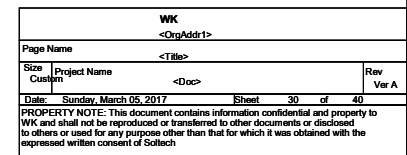
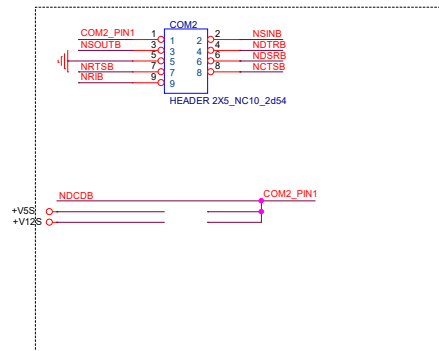
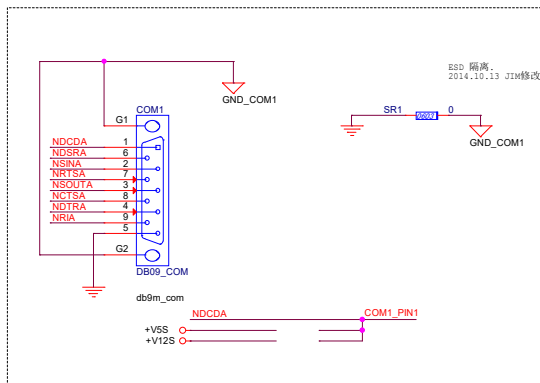




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## Sequencing Rails Within The Same Well

### Suspend Well Voltage Ramp Up/Down Requirements

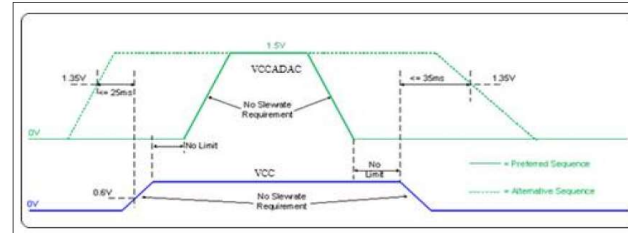
Voltage Rail 1	Voltage Rail 2	Power Up Requirement	Power Down Requirement
VCCSUS3_3	DCPSUS1, DCPSUS2, DCPSUS3	VCCSUS3_3 must be powered up before DCPSUS*, or not more than 0.7V below DCPSUS* while the two rails ramp up.	VCCSUS3_3 must be powered down after DCPSUS*, or not more than 0.7V below DCPSUS* while the two rails ramp down.
VCCSUS	Platform USB Vbus	VCCSUS ramps up before Vbus reaches 1.05V while ramping up.	VCCSUS ramps down after Vbus reaches 1.05V while ramping down.

In external VR mode (Mobile Only), this relationship needs to be met by the platform.  
In internal VR mode, the PCH will meet this timing.

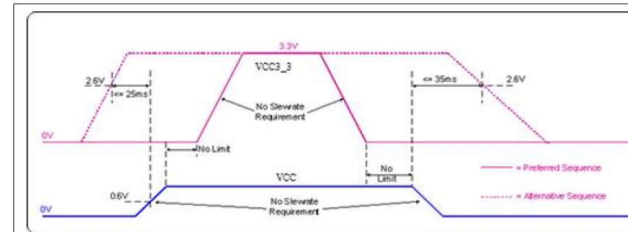
Table 8-34. Core Well Voltage Ramp Up/Down Requirements

Voltage Rail 1	Voltage Rail 2	Power Up Requirement	Power Down Requirement
VCC (1.05V)	VCC3_3 (3.3V)	Preferred Option: - VCC powers up before VCC3_3 Alternative Option: - VCC3_3 may power up before VCC, but VCC must ramp up to 0.6V within 25ms of VCC3_3 ramping to 2.6V.	Preferred Option: - VCC powers down after VCC3_3 Alternative Option: - VCC may power down before VCC3_3, but VCC3_3 must ramp down to 2.6V within 35ms assuming a linear ramp.
VCC (1.05V)	VCC1_5 (1.5V) Note 1, 2	Preferred Option: - VCC powers up before VCC1_5 Alternative Option: - VCC1_5 may power up before VCC, but VCC must ramp up to 0.6V within 25ms of VCC1_5 ramping to 1.35V.	Preferred Option: - VCC powers down after VCC1_5 Alternative Option: - VCC may power down before VCC1_5, but VCC1_5 must ramp down to 1.35V within 35ms assuming a linear ramp.

### Sequencing Requirements between PCH VCC1\_5 and VCC Core Rail



### Sequencing Requirements between PCH VCC3\_3 and VCC Core Rail

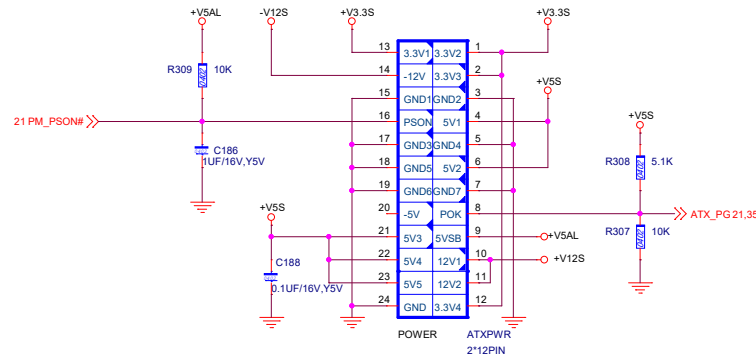


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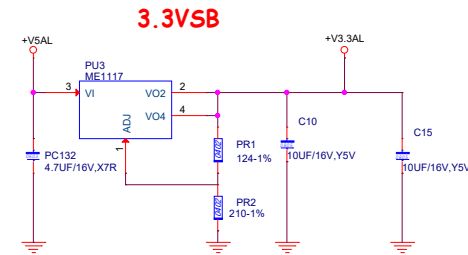
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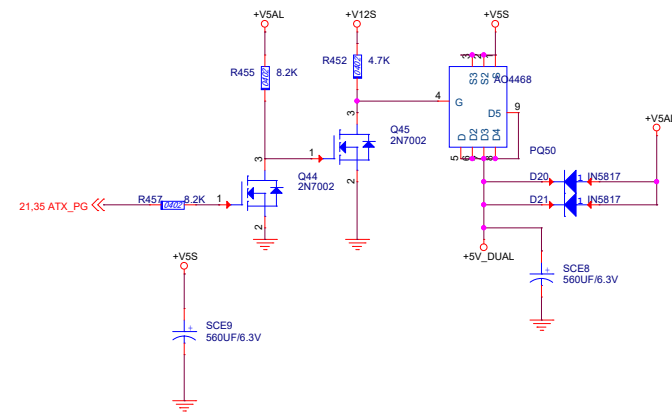
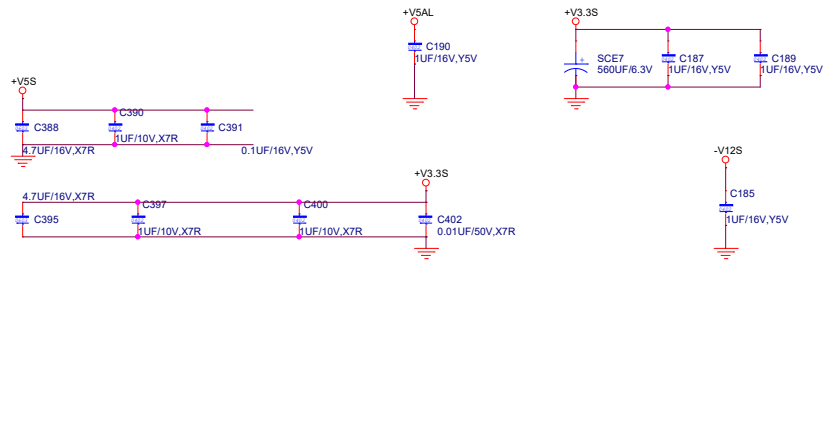
# ATX POWER CONNECTOR



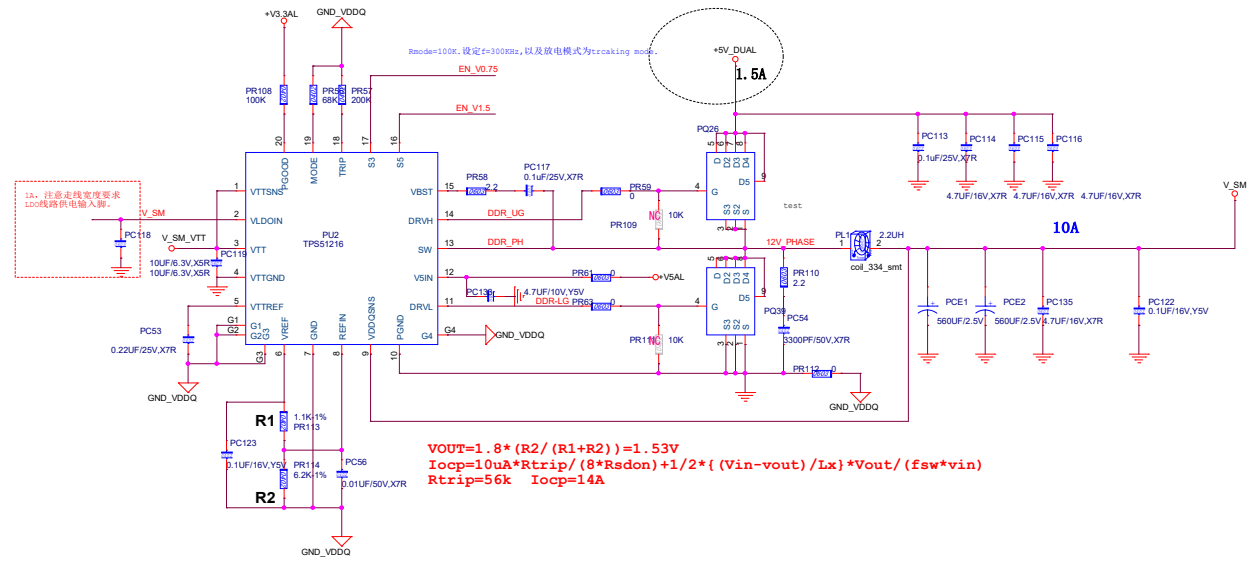
# 5VSB转3.3VSB



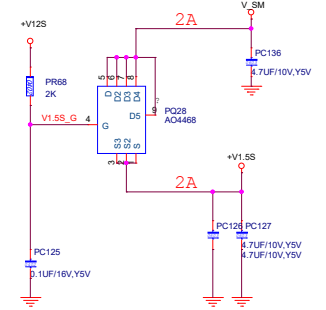
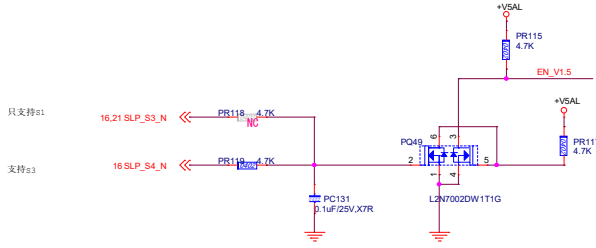
# 5V DUAL



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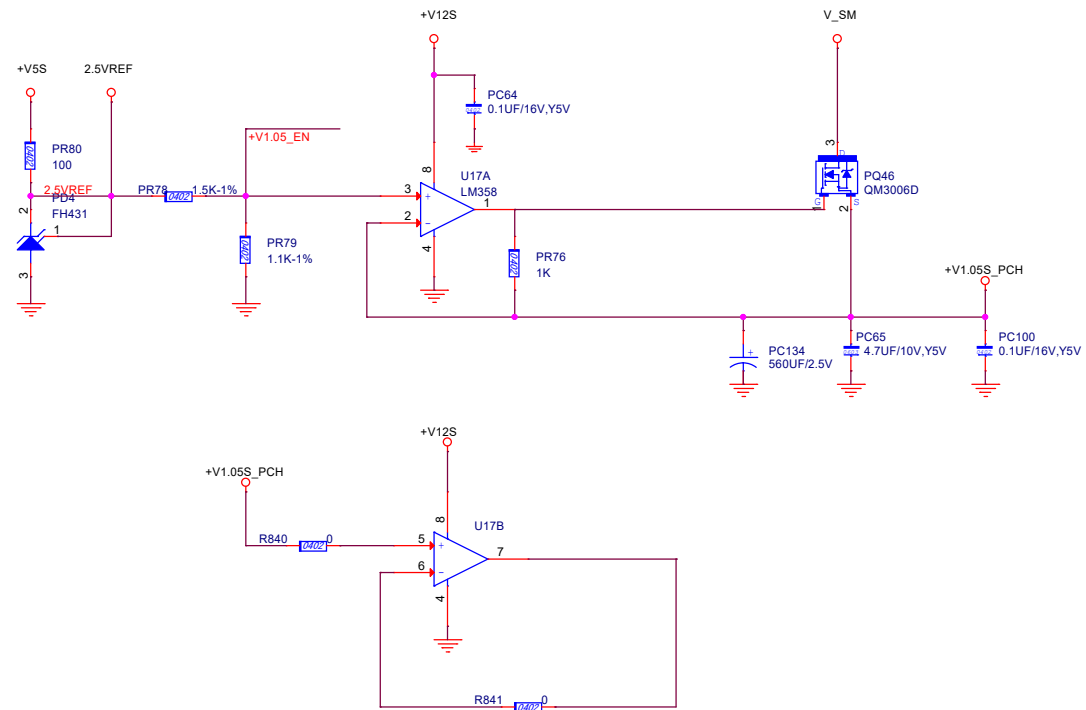
$V_{OUT} = 1.8 * (R2 / (R1 + R2)) = 1.53V$   
 $I_{OCP} = 10uA * R_{TRIP} / (8 * R_{SDON}) + 1/2 * \{ (V_{IN} - V_{OUT}) / L_x \} * V_{OUT} / (f_{SW} * V_{IN})$   
 $R_{TRIP} = 56k \quad I_{OCP} = 14A$



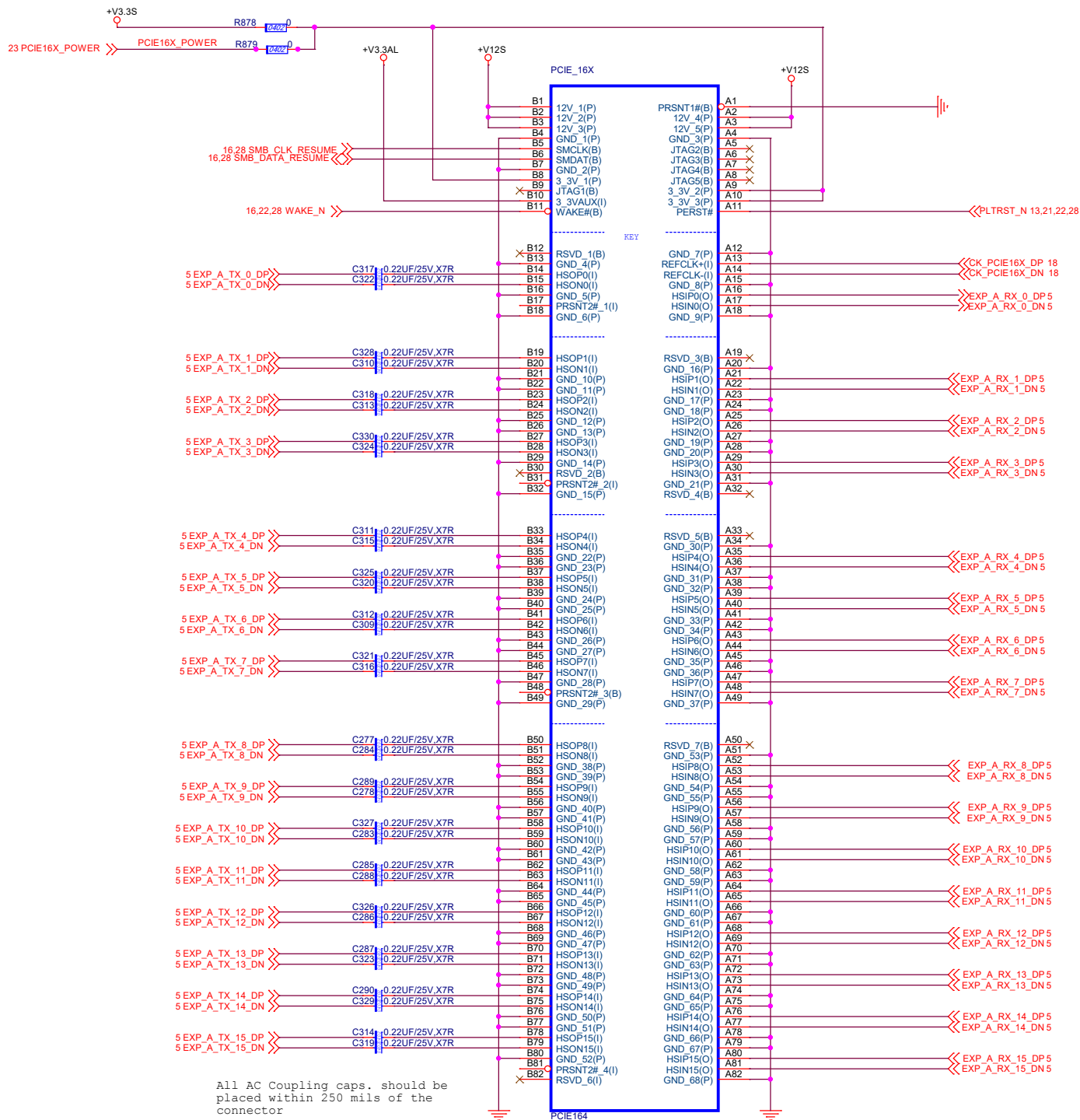
COM用的负12V



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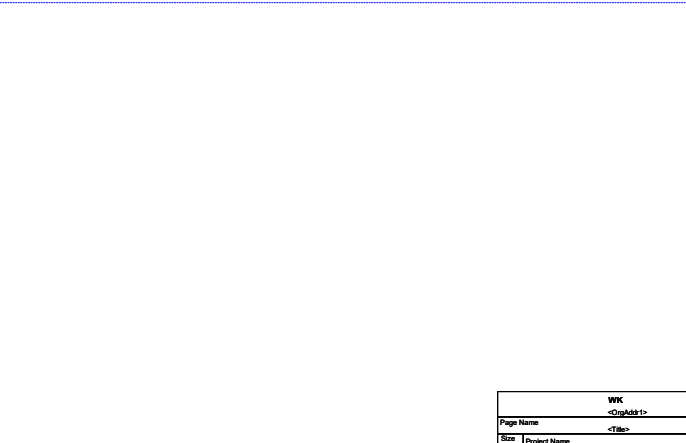
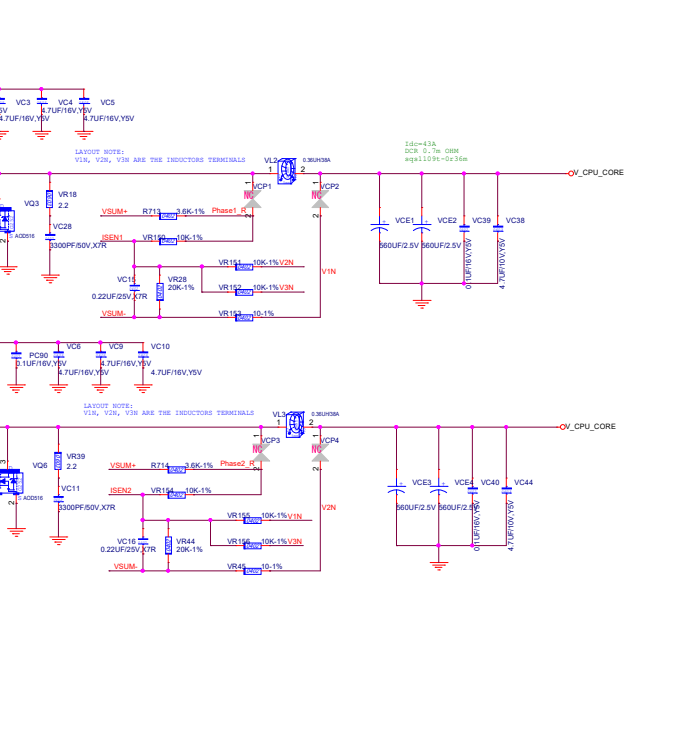


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All AC Coupling caps. should be placed within 250 mils of the connector

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